CLAIMS

Please amend the claims as follows.

1. (Currently amended) A semiconductor integrated circuit comprising:

a plurality of data output pins divided in at least two groups of data output pins;

a data processing circuit to generate output signals responsive to an input signal; and

an output selection circuit with at least a normal mode and a test mode;

where a first group of output signals are provided to a first group of data output pins [[in]]during a first test cycle of the test mode;[[and]]

where a second group of output signals are provided to the first group of data output pins during a second test cycle of the test mode; and

where during the normal mode:

the first group of output signals are provided to the corresponding data output pins of the first group of data output pins; and

the second group of output signals are provided to the corresponding data output pins of a second group of data output pins.

2. (Original) The semiconductor integrated circuit of claim 1 where the output selection circuit repeats the first and second test cycles during testing.

3. (Previously presented) The semiconductor integrated circuit of claim 1

where the output selection circuit sends odd output signals to odd data output pins during the first cycle of the test mode; and

where the output selection circuit sends even output signals to odd data output pins during the second test cycle of the test mode.

4. (Previously presented) The semiconductor integrated circuit of claim 1

where the output selection circuit sends odd output signals to even data output pins during the first cycle of the test mode; and

where the output selection circuit sends even output signals to even data output pins during the second test cycle of the test mode.

5-6. (Canceled)

7. (Currently amended) A method for outputting data during a test mode of a semiconductor integrated circuit having a plurality of data output pins divided in at least two groups of data output pins, the method comprising:

sending some output signals to a first group of the data output pins during a first phase of the test mode;[[and]]

sending remaining output signals to the first group of the data output pins during a second phase of the test mode;

sending the some output signals to the corresponding data output pins of the first group of the data output pins during a normal mode; and

sending the remaining output signals to the corresponding data output pins of a second group of the data output pins during the normal mode.

8. (Previously presented) The method of claim 7 where the sending some output signals and the sending remaining output signals are repeated during the test mode.

9. (Previously presented) The method of claim 7 where sending some output signals includes sending an ith output signal (i being a positive integer) to an ith data output pin.

10. (Original) The method of claim 9 where i is a positive odd integer.

11. (Previously presented) The method of claim 9 where sending remaining output signals includes sending an (i+1)th output signal (i being a positive integer) to an ith data output pin.

12-15. (Canceled)

16. (Previously presented) The semiconductor integrated circuit of claim 1 where the output selection circuit is adapted to send all output signals to corresponding output pins during the normal mode.

17. (Previously presented) The method of claim 9 where i is a positive even integer.

18. (Previously presented) The semiconductor integrated circuit of claim 1,

where the plurality of data output pins are divided in at least two groups of data output pins, including the first group of data output pins; and

where the first group and the second group of output signals are not provided to a second group of data output pins during the first test cycle and the second test cycle of the test mode.

19. (Canceled)

20. (Previously presented) The method of claim 7, where the plurality of data output pins are divided in at least two groups of data output pins including the first group of data output pins, the method comprising:

not sending the some output signals and the remaining output signals to a second group of data output pins during the first phase and the second phase of the test mode.

21. (Canceled)